

SemiCon Times

March 7th 2010

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*Time to test your
Verilog, VHDL modeling
and Digital Design
techniques*

Are You Industry Ready? Test it yourself!!

Verilog Questions - Timing

1. What is time period and what is duty cycle? How can you model two clocks of 75% and 25% duty cycle using the same time period?
2. What are setup and hold time? How do you model them in verilog? Give examples.
3. What does 'timescale directive do in verilog? Given a timescale of 1ns/100ps what would be the time in which simulation results would show up?
4. Explain the difference between following verilog code lines?

```
#5 a = b;  
a = #5 b;
```
5. Explain the difference in a latch and a flip flop using their timing waveform?

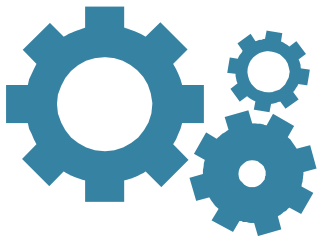
VHDL Modeling Questions

1. What are the various design units in VHDL? Comparing with Verilog, why were the VHDL DUs created in this manner?
2. What is the practical use of a for-generate statement?
3. Give an example to show the difference between an inertial and a transport delay assignment statement.
4. What is the need for a record type in VHDL?
5. When you assign to a VHDL signal array slice inside a process, what happens to the rest of the signal?

Digital Design Questions

1. Can integer DIVIDE operation be performed in a fixed number of cycles?
A. NO **B. YES**
2. What is the function of a barrel shifter? For which arithmetic operation is it used?
3. Why does the static power consumption of CMOS logic with same operating condition go up with shrinking geometry (ex: 120 nm to 90 nm)?
4. What is the gate complexity of the fastest n-bit integer multiplier
A. $O(n)$
B. $O(n \cdot \log n)$
C. $O(n^2)$
5. Which logic function can be used to prioritize n interrupt sources?
A. n-input MUX
B. n-input decoder
C. n-input encoder
D. n-input priority encoder

*Get yourself
Registered for Summer
Training before all the
seats are taken!!
Act Fast!!*



Summer Training 2010 – Registrations Open

Registration for Summer Training -2010 is open now. The summer training is available in three different domains:

1. **Summer Training in VLSI Design**
2. **Summer Training in Embedded Systems Design**
3. **Summer Training in Software Development**

For Details please visit http://designkop.org/summer_intrenship.php

Attractive Early Bird Offers

Upcoming Technology – DFT Part II

What is DFT?

To understand DFT further, we will start with one of the most basic aspects of circuit testing - modeling faults.

We will start with the simplest of models - the stuck-at faults.

Let us start with an and-gate. In this device, as we well know, a zero at any input produces a zero output; and only ones on both outputs produce a one at the output. Suppose, due to some manufacturing defect, the output of the and-gate is permanently stuck at a zero state. How do we test for this? It is easy to see that we must attempt to drive the output to a state which is different from the stuck-at value. This is done by setting both inputs to '1'. Now, if/when we see the output at '0', we know the gate is faulty, and the fault is that the output (or one or both of the inputs) is "stuck-at 0". Giving any other value on the two inputs will not expose the stuck-at-zero fault.

How does one expose a "stuck-at-1" fault for an and-gate. Any of the following inputs will suffice - "0,1", "1,0", "0,0", because we will expect to see a '0' at the output, but will see a '1'.

How about an or-gate, and a "stuck-at-0" fault at the output? Well, any of the following inputs exposes this fault - "0,1", "1,0", "1,1". And a "stuck-at-1" at the output? This can be exposed by exciting the gate with a "1,1" input.

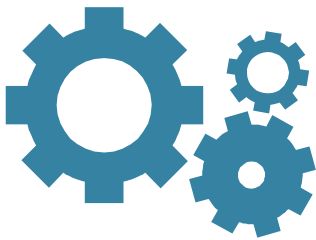
What do we infer from the above?

1. Each kind of simple faults - stuck-at-0 or stuck-at-1 - can appear at any of the inputs or output lines of a gate or network of gates.
2. Depending on the gate logic, each fault requires a separate input string (or input vector) to expose or excite that particular fault.

An exercise for you - take other kinds of gates, and for various stuck-at faults, on either the input or output lines, work out what input vectors will excite that fault.

You can send your answers to vlsi@designkop.org.

Simple faults like stuck-at-0 and stuck-at-1 can appear at any of the inputs or output lines of a gate or network of gates



Industry Watch – SemiCon Ecosystem in India

In the previous three editions of the newsletter, we covered the three biggest EDA companies - **Cadence, Mentor and Synopsys**.

There are other excellent EDA companies worldwide, and some of them have their offices in India too. The following list includes companies that create tools or solutions in support of hardware design **Calypto Design Systems, Apache Design Solutions, Atrenta, Denali Design Systems, CoWare, EVE Design Automation, Sasken, Softjini, Virage Logic, TranSwitch, Synfora, ARM Embedded Technologies, etc.**

The above list includes companies that create libraries in aid of design, or provide tools and utilities. The dividing line between EDA companies and fabless design companies begins to blur, since some of the big EDA companies also create component libraries for microprocessor, ASIC and board design.

In future editions, we will cover some of these companies, and point out how they function, including how the fabless design companies uniquely straddle the space between design and design automation.

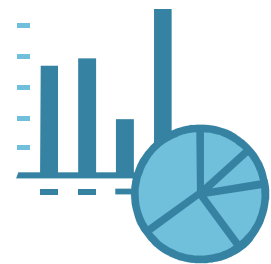
In addition, India is host to the **major FPGA companies of the world - Xilinx, Altera and Actel**. These companies design, fabricate and sell FPGAs. An interesting fact is that most of them also provide the tools required by designers to design systems using these FPGAs, so they also have a considerable amount of EDA tool development being done inside their companies.

The pride of place naturally goes to the design companies themselves, of which almost all the top companies of the world have an India presence. Below is just a very small and partial list **Vitesse, SanDisk, Tensilica, Rambus, Qualcomm, QLogic, PMC, Sierra, NXP Semiconductors, NEC Electronics, Moschip Semiconductor Technologies, Marvell Semiconductor, LSI, KLA Tencor, Kawasaki Microelectronics, Ittiam, Intel, Infineon, IBM, Freescale, Delphi Automotive Systems, Cypress, Conexant, Broadcom, Alcatel, AMD, Analog Devices, Applied Materials, STMicroelectronics, Texas Instruments, Tejas Networks, TSMC, Toshiba, Samsung, etc.**

As you can see, the whole ecosystem of companies that are involved in design are represented in India.

At DKOP, we work with several of them, and attempt to keep an ear to the ground, getting to understand their requirements, of people, and skills that those people should have.

In our future editions, we will come back to cover these companies one by one, pointing out each company's unique requirements of knowledge, skills and experience.



Mock Interviews

Details are provided again on popular requests!!!

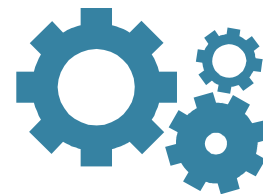
Venue: Campuses/DKOP office

Eligibility: BE/BTech/ME/MTech/MSc students and graduates in ECE, EE, EI, CS, CE, MCA and allied fields

Offerings

1. **Quick Interview:** duration 1 hour - this will be a purely technical interview. A SWOT analysis will be provided to the student within 24 hours.
Cost: Rs 750/- per person (Rs 500/- per person for groups 10 plus students)
2. **Interview + Review:** duration 1 hour + 1 hour (after 2+ weeks) - A follow-up will be done after 2 weeks, to cover the indicated areas.
Cost: Rs 1000/- per person (Rs 700/- per person for groups of 10 plus students)
3. **Extended Interviews:** This is to approximate the more stringent interviews done at some top companies. Duration - 5 hours - 5 sessions of 1 hour each, 4 technical and 1 HR.
Cost: Rs 2500/- per person (Rs 2000/- per person for groups of 10 plus students). A detailed review feedback will be provided.
4. **Extended Interviews with follow-ups** after 2+ weeks.
Cost: Rs 3500/- per person (Rs 3000/- per person for groups of 10 plus students)
5. **Group Interviews** – Individual SWOTs will NOT be done. A group-wise SWOT will be provided.
Group of 5: 2 hours - Rs 1750/- per group (Rs 350/- per person)
Group of 10: 2 hours - Rs 2000/- per group (Rs 200/- per person)

*Get yourself Industry
Ready for building a
career in core industry*



For Working Professionals: All the four offerings, that is, 1 to 4, are offered to working professionals also. There's no group discounts for working professionals and the venue will be DKOP office only. The costs of each of the offerings are categorized below:

- A. Years of experience: 1-5
1. Rs 1500/-
 2. Rs 2500/-
 3. Rs 5000/-
 4. Rs 7500/-
- B. Years of experience: 6-15
1. Rs 3000
 2. Rs 5000
 3. Rs 10000
 4. Rs 15000
- C. Years of experience: 15+
1. Rs 5000
 2. Rs 8000
 3. Rs 20000
 4. Rs 30000

News & Updates

1. January chip sales increase 0.3 percent from December

Source: SIA, March 1 2010 www.sia-online.org

The Semiconductor Industry Association (SIA) today reported that worldwide semiconductor sales in January were \$22.5 billion, an increase of 0.3 percent from December sales of \$22.4 billion. ***Sales increased by 47.2 percent from January 2009 when sales were \$15.3 billion.*** All monthly sales numbers represent a three-month moving average.

2. Defence offers opportunities to Indian electronics

Source: EETimes, March 1 2010 www.eetindia.co.in

For the first time ever in an electronics exhibition in India top defence officials came together to share the opportunities with private companies to serve the needs of indigenisation and transfer of technology. The event was the Electronics Next India 2010 exhibition for EMS, electronic components, production and materials which was inaugurated by director general, EME, Lt. General AKS Chandele PVSM, AVSM. Speaking on the occasion he said "This year's edition puts a spotlight on defence and strategic electronics and [the defence industry] has launched a series of initiatives to encourage and invite private firms to work in the field of defence electronics.

Learning Resources on the Internet

We spend hundreds of hours wandering about the Internet, often losing our way in search of something trivial. Do you remember those times, when, looking for something, you got trapped into following endless link after link, and looked up hours later in dismay, to realize that you were nowhere nearer the objective.

For inquiring minds, one trove of treasure is MIT's Open Courseware, available at <http://ocw.mit.edu> This has material on more than 1900 courses, taught by the MIT faculty.

Even if you may not have access to the world's best college or its faculty first hand, you can make use of their course-ware, and that too for free.

Any student or teacher can gain tremendously by using these resources to enhance their knowledge.

So, browse, and enjoy!

Upcoming Events

1. The IEEE-SA Corporate Advisory Group will present "**Global Standards at IEEE** " on **9 March 2010 in Bangalore**, India at the Royal Ballroom, Leela Palace Hotel. The seminar is a premier event for those who are involved in the advancement of technology and interested in learning more about the global impact of IEEE standards. Leaders from industry will provide their insight through presentations and case studies on areas such as smart grid, software life cycle, IEEE 802@, and design automation. In addition, the IEEE-SA Corporate Advisory Group will be leading a series of outreach sessions at various locations in Bangalore on 10-12 March. Further information and registration for those outreach sessions can be found [here](#).

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